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A Design Tools Flow and New Architecture for Low-Power Gated-clock Synchronous Controllers

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***Abstract*— Controllers based on Synchronous Finite State Machines (SFSM) are widely used in the design of Embedded Digital Systems (EDS) and can be implemented in Field Programmable Gate Arrays (FPGAs) or VLSI (Very Large Scale Integration). A class little known and very interesting of SFSM in the FPGA or VLSI platforms is the SFSMs of direct output (SFSM_DO). These state machines use the output signals as state signals, thus allowing several advantages when compared to conventional SFSM classes. Of these advantages, we can mention: elimination of glitches in the output signals; reduction of the number of state variables; reduction in latency time. An important requirement in EDS is power consumption. The literature shows that SFSMs with gated-clock have a substantial average reduction in dynamic power. This paper proposes architecture for SFSMs_DO with gated-clock. Through the case study the proposed architecture showed a reduction in the dynamic power of 86.3% when compared with conventional gated-clock SFSMs.**

Keywords—models of machines, genetic algorithm, state assignment

I. INTRODUCTION

An embedded digital system (EDS) can be formed by synchronous controllers and data-paths [1,2]. Can be implemented in FPGA (Field Programmable Gated array) or VLSI (Very Large Scale Integration). An EDS applied in military and aerospace systems have critical requirements, which use decision controllers, which can be highly complex [3]. These controllers can be modeled by synchronous finite state machines (SFSMs). Two important models of SFSMs are the models Mealy [4] and Moore [5] shown in Fig. 1. The SFSMs are described by a state transition graph (STG), where the graph is directed and cyclic, with vertices that represent the states and the edges are state transitions that can be labeled with a transition condition [1].

Figure 2 shows a STG Moore model. In an EDS System the performance and power consumption are very important requirements. The reduction of the energy consumption is one of the most important tasks in the projects of digital circuits.

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It is due to the increasing of portable applications, so as: laptops, notebooks, communication (cellular and so on), satellites and military applications. The controllers of an EDS system have a great contribution to performance as well as energy consumption.

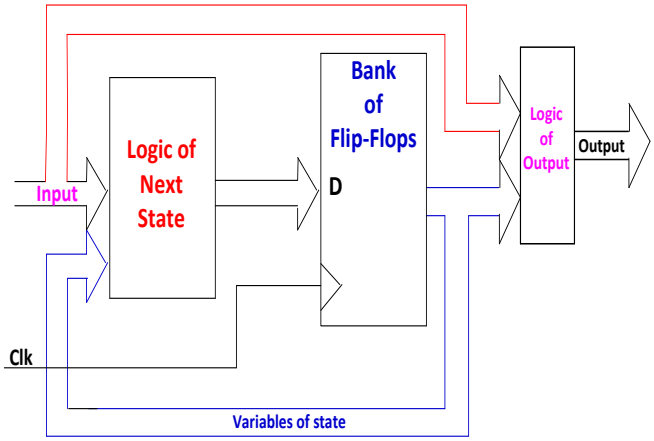

Fig. 1. Synchronous FSM: Mealy or Moore models.

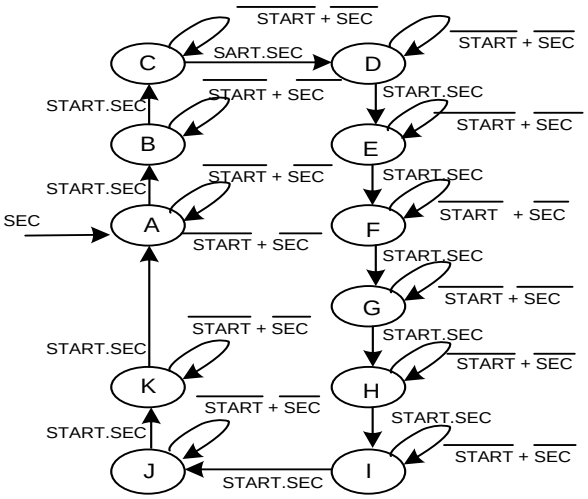

Fig. 2. STG specification Moore model of a Timer of [1].

Traditionally, digital circuits are implemented with components that are built with CMOS technology. The power dissipated in the CMOS components follows the following expression [6]:

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$$P_{TM}=1/2.C.V^2_{DD}.f.N + Q_{sc}.V_{DD}.f.N + I_{fuga}.V_{DD} \quad (1)$$

Where: P_{TM} is the average total power dissipated, V_{DD} is the supply voltage, f is the operating frequency, the N factor is switching activity, i.e. the number of transitions at the output of a gate, and the factor Q_{SC} and C are respectively the amount of charge and the capacitance [6]. Equation *1* is composed of the dynamic, quiescent and static powers. Equation 2 describes the dynamic power, where it is responsible for more than 80% of total power consumption under certain working conditions [7].

$$P_{DYNAMIC}=1/2.C.V^2_{DD}.f.N \quad (2)$$

Dynamic power reduction techniques are applied at different levels of the digital design [7]. In the synthesis of synchronous controllers the power reduction proposals are being made at the logical level, which are: logic control of clock [8,9], Flip-Flops that act on the two edges of the clock transition [10], decomposition [11,12], state assignment [12,13] and logical minimization [14].

In a digital system, the sequential part is the major contributor to power dissipation. Recent studies indicate that the clock of these systems consumes a large percentage (15% to 45%) of the power of the system [7]. Thus, the power of the circuit can be greatly reduced if it reduces clock activity. In the above proposals, the gated-clock control (GCC) that inhibits the clock signal in the self-transitions has obtained expressive results in the reduction of the dynamic power (see section II). The architectures for synchronous controllers that using GCC proposed in [8,9], are based on the Moore model and states are defined only by state variables. Pomeranz [15] describes a new model of SFSM called SFSM of direct output where the variables of output are used as state variables (SFSMs_DO - see Fig. 3). SFSM_DO has several advantages over conventional SFSM, especially when implemented in FPGAs.

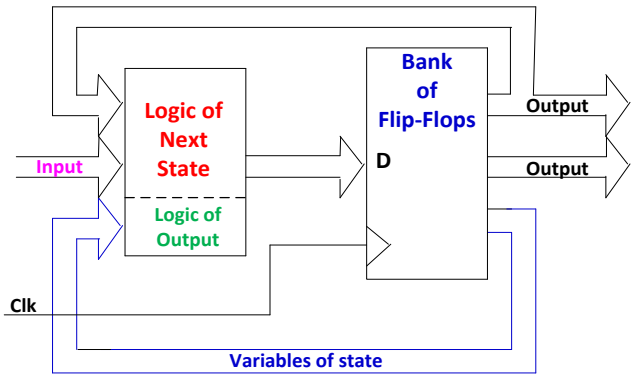

Fig.3 Synchronous finite state machine with direct output.

In this context, this paper proposes a new architecture shown in Fig. 4 for low-power SFSMs that uses output variables as state variables. The new architecture use transparent D latches to store states and inhibits the clock signal in the GCC style. Transparent latches are used as master slave flip-flops, but differ from conventional configurations, the next-state and output logic are between master and slave latches. This configuration reduces the propagation of glitches, which reduces dynamic power. Figure 4 shows the proposed architecture where the clock inhibition logic for the self-transitions acts in series with the next-state and output logic and inhibits the clock signal in both master latches and slave latches. We also propose a flow of design tools for the automatic synthesis of SFSM_DO with gated-clock. Through a case study we show the high reduction in dynamic power of the proposed architecture.

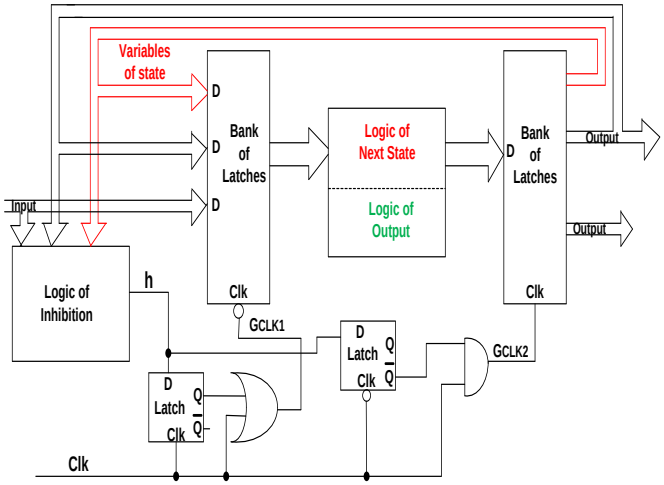

Fig.4 SFSM_DO based on latches with gated-clock.

II. ARCHITECTURES FOR SFSM: OVERVIEW

A. *SFSM of Direct Output*

McCluskey [16] was the first to propose the use of the output and input signals of an FSM to compose the description of internal states. The choice of the minimum number of input and output signals for encoding is an NP-hard problem. Later, Pomeranz [15], elaborates an algorithm that combines the values of the signals of input and output that can be used in the codification of the internal states. Forrest [17] proposed an algorithm that uses the values of the output signals of FSM model Moore as the initial code of the internal states. Solovjev [18] proposed structural models of FSMs based on the architectural capabilities of FPGAs, where these models make it possible to use the values of the signals of input and output of a FSM as internal state codes. Klimowicz et al. [19] proposed a model that combines the Moore and Mealy models to use output signals in state encoding, but without increasing internal states. Solov'ev [20] proposes a method involving two phases, first splitting the internal states of the FSM (to satisfy the necessary conditions for the construction of the FSM_DO class) and encoding the internal states (to ensure that the codes are mutually orthogonal).

For the SFSM_DO class, the models are called Moore Direct and Mealy Direct which are variants of the traditional Moore and Mealy models [4,5]. On Moore's direct machines the code of the output signals coincides with the state code. In direct Mealy machines the code of the output signals coincides

with the code of the next state. There are four advantages to using the output signals as state signals: *1)* Reduction or elimination of state variables, therefore, may have area reduction; *2)* In the classic implementation of the Moore model machines there are three blocks (excitation logic, flip-flops and output logic), but in direct Moore model machines there are only two blocks (excitation logic and flip-flops), so there is a reduction In latency time; *3)* Output signals are free of glitches, so there is a reduction in switching activity and can be used to activate counters and registers (Data-path); *4)* Reduction or elimination of state variables increases the observability and controllability of the circuit, thus facilitating testability.

B. *Clock logic control*

Among the solutions proposed for reducing the dynamic dissipated power of the synchronous controllers, the GCC control is very interesting.

This strategy uses an additional logic to disable the clock in the states with self-transition (*self-loop*). For some FSMs, most clock cycles are used in states with self-transition. In these states there is also dynamic power dissipation because the flip-flops (FFs) change state internally, although no changes occur at the FFs exit. Figure 5 shows the target architecture for synchronous controllers with clock inhibition, as proposed in [8].

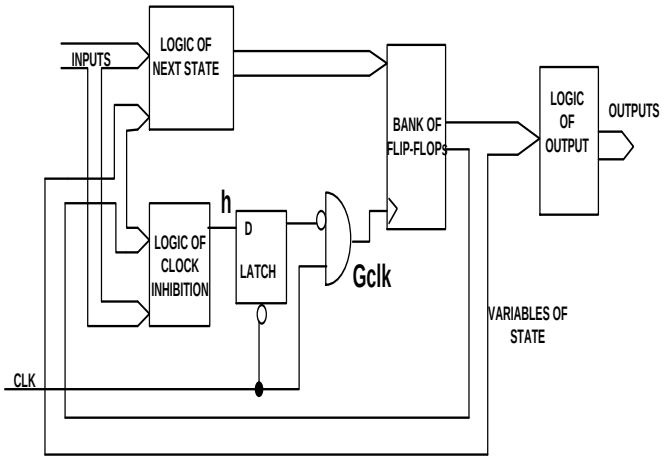

Fig.5. Proposed of SFSM with gated-clock of [8].

III. SYNTHESIS OF SFSM_DO WITH GATED-CLOCK

The proposed flow design synthesizes the SFSMs_DO with gated-clock in the target architectures shown in Fig. 4; it is defined in three steps and start from the STG specification:

1. Realize the state assignment using SAGADOM tool [21]. This tool suitable for SFSM_DO does state assignment using genetic algorithm and generates a conflict-free STG (FC_STG).
2. Generate in the Kiss2 format the FC_STG specification and the state transition table of the inhibition function (STT_FI) [22].
3. Starting of the FC_STG specification and SST_FI in formats kiss2, synthesize the SFSM_DO with gated clock, using a logic minimization conventional tool, ESPRESSO of [22], obtaining the equations of the output signals and if there are the equations of the state signals, as well as the inhibition function *h*.

IV. CASEY STUDY

In order to illustrate the proposed architecture for the SFSMs_DO with gated-clock, it was applied in STG specification of Fig. 6a. The first step is to realize state assignment, which verifies the occurrence of conflicts [21]. If there are conflicts the solution is the insertion of state variables. The algorithm of the SAGADOM tool inserts the smallest number of state variables to solve the conflicts. By doing the conflict analysis of STG specification of benchmark in Fig. 6a, Fig. 6b depicts the table of conflicts, (for simplifying reasons, the self-loop transitions were hiding at the conflict table) where "v" means that the state transitions are not conflicting and "x" that they are conflicting. Five conflicts can be seen. To solve the conflicts, the SAGADOM tool [21] has inserted two variables of state, which are *ss0* and *ss1*. Figure 7 shows the STG specification, full satisfying the FC_STG condition on the SFSM_DO architecture.

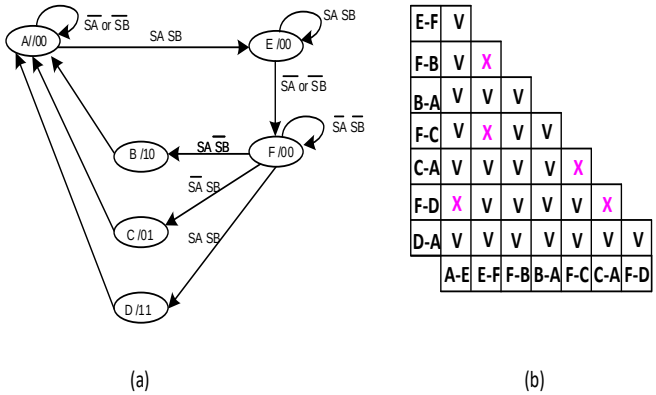

Fig. 6. Conflicts analysis of [21]: a) STG spec. with conflicts; b) table of conflicts.

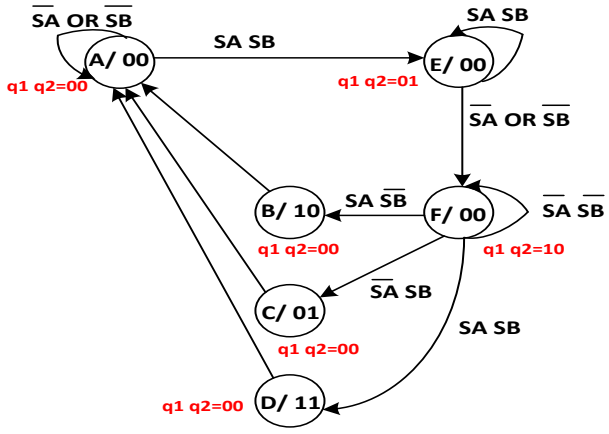

Fig. 7. STG specification free of conflits.

The second step generates the STT_FI table, as shown in Fig. 8 and transforms into the kiss2 formats both STT_FI and FC_STG. The third step generates the next-state, output, and inhibition equations using the ESPRESSO [22] tool. Figure 9 shows the partial logic circuit of SFSM_DO in the architecture of Fig. 4. Figure 10 shows the schematic for GCC of the proposed architecure and Fig. 11 shows the logic circuit of the inhibition function.

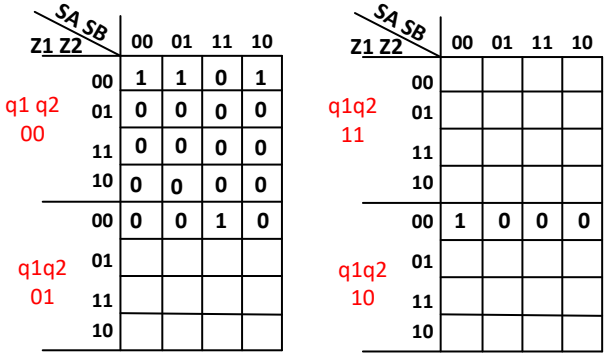

Fig. 8. STT of inhibition function of case study.

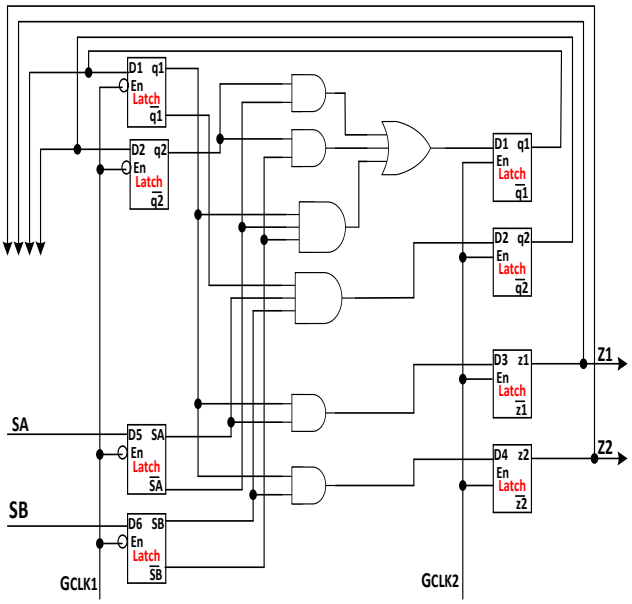

Fig. 9. Equations of next-state and output: circuit logic.

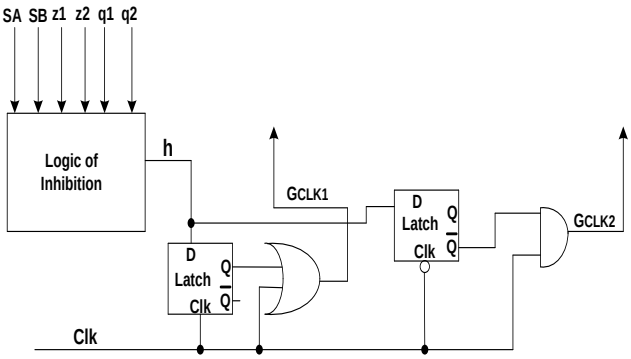

Fig. 10.Schematic for gated-clock control.

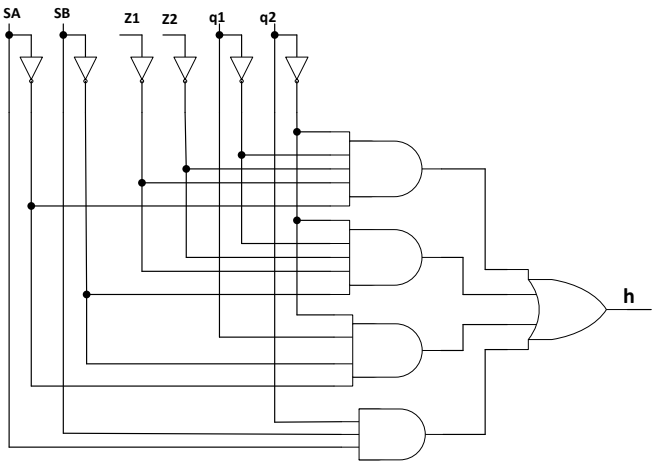

Fig. 11. Inhibition function of clock signal: logic circuit.

V. Simulation & Some Results

To an analysis of the case study, we implemented in four different architectures, which are: a) the proposed architecture, in case Fig. 4; b) one-hot architecture, which is widely used in the FPGA platform; c) classical architecture, Moore model with optimal state assignment; State minimization uses the Stamina [23] tool and the Jedi tool [24] generates optimal state encoding. The four obtained circuits were described in structural VHDL and were simulated and compiled in ALTERA tool, Quartus II software, version 9.1, Cyclone III family, and EP3C16F484C6 device [25]. Figure 12 shows the post-layout simulation of the case study in the architecture of Fig. 4. The waveforms met the specification and no glitch in signals was detected, i.e. if there are glitches in the signals, they do not propagate.

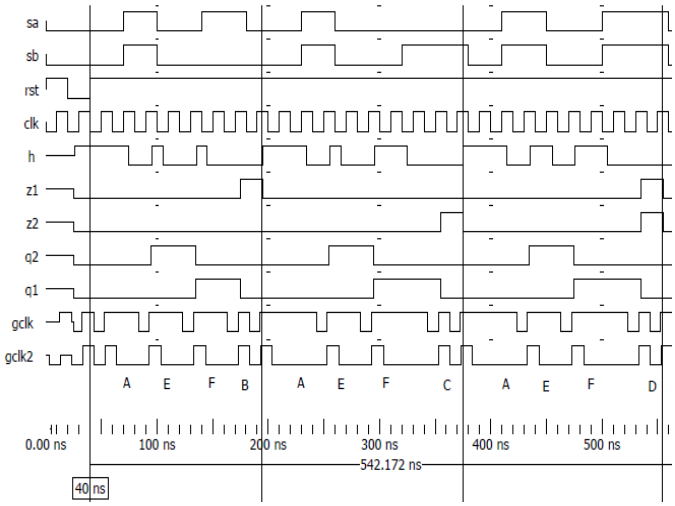

Fig. 12. Simulation of case study with gated-clock.

Table I shows the results of the case study of four implementations, which are latency time, maximum clock rate, dynamic power and area, in the case number of LUTs and FFs in FPGA platform. Analyzing table I, we have the following results: When compared to SFSM with GCC of Fig. 5 we obtained a reduction in the dynamic power of 86.3%. As

compared with SFSMs of coding one-hot and optimized, the performed by the Jedi tool [24], we obtain a 95.2% reduction in dynamic power. When compared to the other three architectures, we obtained in the clock rate an average increase of 14.7% and an average area penalty (LUTs + FFs) of 67%. In the latency time the times were relatively equivalent. Table II shows results of the logical minimization, in the case the equations Booleans of the next state, output and inhibition. Comparing with the three architectures, we obtained a mean equivalence in products and an average penalty of 14.8% in literals.

TABLE I. COMPARISON BETWEEN ARCHITECTURES ON FPGA

	Freq-MAX	Latency (ns)	Area (LUTs+FFs	Dynamic Power (mw)
Moore-Fig.1	146MHz	4.7ns	**4**+4	4.75mw
Moore-One-Hot	142MHz	5.0ns	7+6	4.75mw
GC-FSM-Fig.5	146MHz	**4.6ns**	9+4	1.72mw
Proposal-Fig.4	**166MHz**	4.7ns	19+**0**	**0.23mw**

TABLE II. COMPARISON BETWEEN ARCHITECTURES ON VLSI

	Nro. Products	Nro. Literals	Nro. Flip-Flops
Moore-Fig.1	**8**	**22**	4
Moore-One-Hot	10	26	6
GC-FSM-Fig.5	12	33	4
Proposal-Fig.4	10	31	**0**

VI. CONCLUSION

The SFSMs_DO have interesting features when compared to SFSMs in the classic Moore and Mealy models. These characteristics, such as output signals have no glitches and reduced latency time, are relevant on the FPGA and VLSI platforms. This paper proposed new architecture for low-power SFSMs_DO. It uses transparent D latches to memorize states and the clock signal is inhibited in the auto-transitions. For a case study, the new architecture achieved a high reduction in dynamic power. For future work, to apply in a large set of benchmarks, to better evaluate its performance and develop a tool for automatic synthesis, generating as output a structural VHDL.

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